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The Verilog Golden Reference Guide is a compact quick reference guide to the Verilog hardware description language, its syntax, semantics, synthesis and application to hardware design. The Verilog Golden Reference Guide is not intended as a replacement for the IEEE Standard Verilog Language Reference Manual.

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The SystemVerilog Language Reference Manual (LRM) was specified by the Accellera SystemVerilog com-mittee. Four subcommittees worked on various aspects of the SystemVerilog 3.1 specification: — The Basic/Design Committee (SV-BC) worked on errata and extensions to the design features of System-Verilog 3.1.

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